Detector Support Group

Weekly Report, 2019-08-28

Summary

Hall A – Super BigBite Spectrometer (SBS) HCAL

- Cut and terminated 96 BNC to LEMO cables.

Hall B – Magnets

- To solve issues with the duplicate/missed timestamps for the data transfer from the FastDAQ cRIO to EPICS the LabVIEW code has been modified.
  - ✶ Found new modified LabVIEW code has significantly less jitter, but at the expense of completely missing a sample.
    - ▪ Most Root files analyzed have 0 timestamp issues.
  - ✶ A slower ADC read rate would eliminate all timestamp issues independent of the LabVIEW code.

Hall B – Gas Control Systems

- NI closed the ticket for the rebooting cRIOs issues since they can't replicate it and they've been running for a month or so without issue.

Hall B – BONuS Target

- Ordered pressure sensors after approval from DA & system owner.

Hall B – GEM

- Created Top View of *GEM Gas Distro* Rack
- Created interior unfolded view showing gas tubing runs inside the *GEM Gas Distro* Rack

Hall B – SVT

- Updated SVT HV deadbands for all the HV currents channels.
  - ✶ Changed from 0.05 to 0.005 nA.

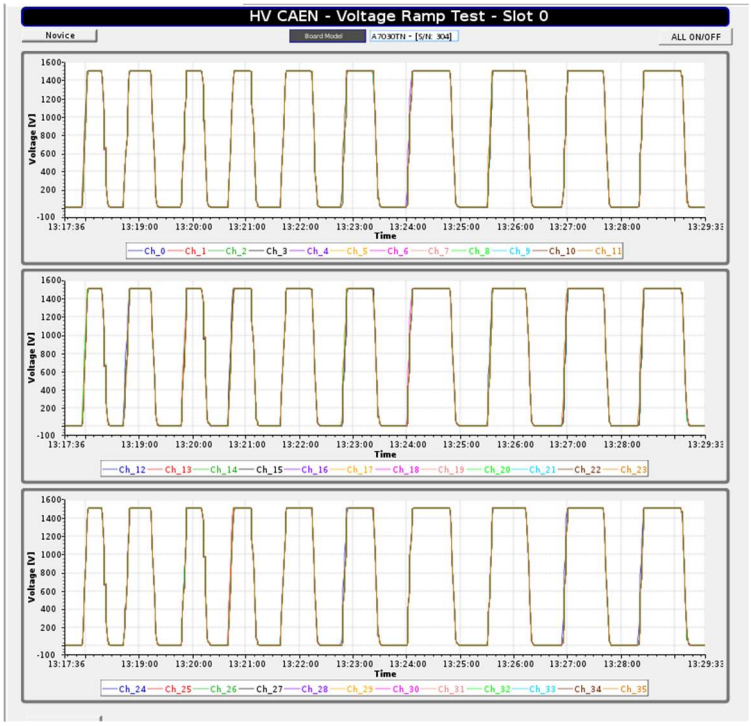
Hall C – CAEN HV EPICS Test Station

- Conducted meeting to present the findings and issues faced during the tests of the SY4527 Systems to CAEN support.
- Tested CAEN A7030 HV board via Secure Shell connection.
  - ✶ Tested all 36 channels under the following specifications:

Voltage Ramp Up/Down Test				
Mainframe Model	SY4527	**Set Voltage**		1500 V
Mainframe S/N	400	**Ramp Up/Down Rate**		250 V/s
Board Models	A7030TN	**Max Current Set**		1000 uA
Board S/N	304	**Load:** 0 Ω	**Vmax:** 1800 V	IMon: ~ 0 uA
Total Channels Tested	36	**Total # Ramp Up/Down per channel**		10/10

  - ✶ Enabled CAEN EPICS Server, and run *Voltage Ramp Test* CSS-BOY screen to only monitor voltage readouts, all parameters were set and control from the Secure Shell Connection interface.

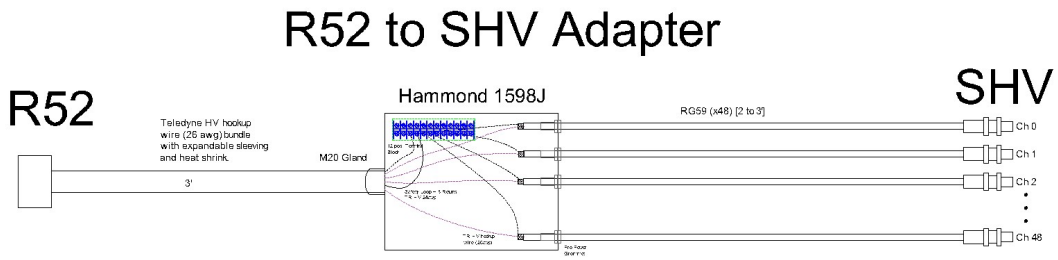
- None of the 36 channels had issues during the test.



Voltage Ramp Test – Slot 0 CSS-BOY screen shows ten ramp up/downs with no issues

Hall C – CAEN HV Hardware Test Station

- Completed design and procurement for *Radiall 52* to SHV adapter.



- Continued with testing of A7030TN HV boards.
- Generated CAEN SY4527 Test Station layout in Visio.

DSG R&D – cRIO Test Stands

- Completed testing of NI-9871 RS485 Serial module
- Developed program to test NI-9401 TTL input/output module.
  - Program has two parts:
    - cRIO FPGA: generates clocking based on user-input frequency and reads digital input channels to calculate frequency of detected square wave signal.
    - cRIO Real-Time OS: passes test parameters to FPGA and displays frequencies measured by input channels.

DSG R&D – LV Chassis FPGA

- Unsuccessfully attempted to install Debian and Scientific Linux on SoC; basic Altera-provided Linux console re-installed.
  - ✶ Other distributions would be more up-to-date and allow easier programming of SoC.
- Attempted to modify and compile FPGA program, for example FPGA-SoC program provided by Altera.
  - ✶ Tutorial appears to be missing steps, unable to configure memory mapping between FPGA and SoC.
  - ✶ However, the pre-compiled examples were able to be downloaded and run without issues on board.

DSG R&D – PLC Test Station

- Installed Factory Talk View Version 8 in *dsgwin10* PC.
- Testing RTD PLC module in progress
  - ✶ Wrote a PLC program to read temperature values from RTD temperature sensor.
    - ▪ Temperature readouts are average.
    - ▪ Created four different alarms that trip if the temperature reaches and stays at or above a specified temperature.